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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/602,066	06/24/2003	Satoshi Matsuda	008312-0304355	1198

909 7590 07/13/2006

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EXAMINER	
LOKE, STEVEN HO YIN	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 07/13/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/602,066	MATSUDA ET AL.	
	Examiner	Art Unit	
	Steven Loke	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 April 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2,5,6,8,10,24 and 25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2,5,6,8,10,24 and 25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 10/101,950.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. Claims 2, 5, 6, 8, 24 and 25 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 2, lines 12-13, the phrase "an edge portion of the gate electrode side of the first diffusion layers being located outside of a side surface of the gate electrode" is unclear as how a plurality of first diffusion layers has only one edge. It is believed that it should rewrite as "an edge portion of the gate electrode side of each of the first diffusion layers being located outside of a side surface of the gate electrode".

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 2, 5, 6, 8, 24 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Maruo in view of Shell et al.

In regards to claim 2, Maruo discloses a semiconductor device in fig. 1. It comprising: (a) a semiconductor substrate [10]; (b) a pair of first diffusion layers ([17, 18, 18a] or [18, 18a]) formed within said semiconductor substrate; (c) a gate insulating film [14, 15] including: (i) a first insulating film portion [14] formed on that portion of said semiconductor substrate which is positioned between said first diffusion layers ([17, 18, 18a] or [18, 18a]), and (ii) a second insulating film portion [15] positioned on an edge of said first insulating film portion, said second insulating film portion having a thickness that is larger than a thickness of said first insulating film portion; (d) a gate electrode [16]

having a first gate portion formed on the first insulating film portion and a second gate portion formed on the second insulating film portion, in which the first and second gate portions are formed of the same material (polysilicon), an edge portion of the gate electrode side of each of the first diffusion layers being located outside of a side surface of the gate electrode [16]; (e) a first gate side wall insulating film (a portion of the insulating film [23] extends from the upper right hand corner of the electrode [16] to the lower right hand corner of layer [23]) formed on a side surface of said gate electrode and on a side surface of said second insulating film portion, the first gate side wall insulating film having a first side surface and a second side surface, the first gate side surface being opposite to a side surface facing the gate electrode, the second side surface being opposite to a side surface facing the second insulating film portion, the first side surface being flush with the second side surface.

Maruo differs from the claimed invention by not showing a second diffusion layer formed apart from said first diffusion layers within that portion of said semiconductor substrate which is positioned below said first insulating film portion.

Shell et al. disclose a second diffusion layer [40] formed apart from said first diffusion layers [60, 62] within that portion of said semiconductor substrate [10], which is positioned below said first insulating film portion [20] in fig. 9. Shell et al. further disclose the self-aligned anti-punchthrough implant channels can be formed in the N^- doped substrates for the P-channel FETs by reversing the dopant polarity (i.e., [40] is n-type in a P-channel FET) (col. 7, lines 11-14).

Since both Maruo and Shell et al. teach a LDD-type p-channel MOSFET, it would have been obvious to have the n-type implant of Shell et al. in Maruo because it prevents punchthrough in the channel region.

In regards to claim 5, Maruo further discloses said first diffusion layers further comprises: a pair of extension regions [17] formed below said gate side wall insulating film apart from said second diffusion layer; and a pair of source-drain regions [18, 18a] formed in contact with said extension regions on a side opposite said second diffusion layer.

In regards to claim 6, Maruo further discloses further a second gate side wall insulating film (a portion of the layer [23] extends from the upper right hand corner of the gate [16] to a middle side portion of layer [25a]) formed on a side surface of the first gate side wall insulating film.

In regards to claim 8, Maruo further discloses an interlayer insulating film [23] formed to surround a portion of said gate side wall insulating film, an upper surface of said interlayer insulating film (a portion of layer [23] that has an upper surface coplanar to an upper surface of gate [16]) being coplanar with an upper surface of said gate electrode.

In regards to claim 24, Maruo further discloses an upper surface of the second insulating film portion [15] is positioned higher than a top surface of the first insulating film portion [14], and a bottom surface of the second insulating film portion [15] is positioned lower than a bottom surface of the first insulating film portion [14].

In regards to claim 25, Maruo further discloses a distance between the first diffusion layers [18, 18a] is longer than a gate length of the gate electrode [16].

4. Applicant cannot rely upon the foreign priority papers to overcome the following rejection because a translation of said papers has not been made of record in accordance with 37 CFR 1.55. See MPEP § 201.15.

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claim 10 is rejected under 35 U.S.C. 102(e) as being clearly anticipated by Kim.

In regards to claim 10, Kim shows all the elements of the claimed invention in fig. 2M. It is a semiconductor device, comprising: (a) a semiconductor substrate [300]; (b) a pair of first diffusion layers [312, 314] formed within said semiconductor substrate; (c) a gate insulating film [308, 301b] including: (i) a first insulating film portion [308] formed on a portion of said semiconductor substrate which is positioned between said first diffusion layers, and (ii) a second insulating film portion [301b] positioned on an edge of said first insulating film portion, said second insulating film portion having a thickness that is larger than a thickness of said first insulating film portion; (d) a gate electrode [309a] having a first gate portion formed on the first insulating film portion and a second gate portion formed on the second insulating film portion, in which the first and second gate portions are formed of the same material (polysilicon); (e) a first gate side wall insulating film [313] formed on a side surface of said gate electrode and on a side

surface of said second insulating film portion; and (f) a second diffusion layer [307] (fig. 2D) formed apart from said first diffusion layers [312, 314] within a portion of said semiconductor substrate which is positioned below said first insulating film portion [308]; wherein a conductivity type (n-type) of said second diffusion layer is opposite the conductivity type (p-type) of said semiconductor substrate [300].

7. Applicant's arguments filed 4/27/06 have been fully considered but they are not persuasive.

It is urged, in page 6 of the remarks, that Maruo never discloses an edge portion of the gate electrode side of the first diffusion layers being located outside of a side surface of the gate electrode. However, Maruo does show an edge portion of the gate electrode side of each of the first diffusion layers [17, 18, 18a] being located outside (any area outside the sidewall of the gate electrode [16]) of a side surface of the gate electrode [16]. Therefore, the combination of Maruo and Shell et al. shows all the limitation as claimed in claim 2, 5, 6, 8, 24 and 25.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steven Loke whose telephone number is (571) 272-1657. The examiner can normally be reached on 8:00 am to 5:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on (571) 272-1732. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

sl
July 7, 2006

Steven Loke
Primary Examiner
Steven Loke